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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,621	06/09/2000	Vidyabhusan Gupta	99-LJ-186	3053

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EXAMINER	
ROSALES HANNER, MORELLA I	
ART UNIT	**PAPER NUMBER**
2128	4

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,621	GUPTA, VIDYABHUSAN	
	Examiner	Art Unit	
	Morella I Rosales-Hanner	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2-19-2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1 – 29** have been presented for reconsideration in view of applicant's amended claims.

Response to Arguments

2. Applicant's arguments filed on February 12th 2004 have been fully considered. The Examiner's response is a follows:

2.1 Regarding Applicant's response to the 35 U.S.C. 112, first paragraph rejection of claims 1 –28 as failing to comply with the enablement requirement, Applicant has argued that:

to establish non-enablement, the burden is on the Patent Office to show that a person of ordinary skills in the art cannot make and use the claimed invention "without undo experimentation". Applicant's response [**Pg 11, last paragraph**] has pointed to the specification for the teaching [**Pg 11, lines 5 –10**] of a controller and has pointed out to a well know teaching of a controller.

Applicant's arguments are persuasive therefore the 35 U.S.C. 112, first paragraph rejection based on enablement has been overcome. However, a new rejection for failing to comply with 35 U.S.C. 112, first paragraph based on written description has been applied [please see section 4].

2.2 Regarding Applicant's response to the 35 U.S.C. 103(a) rejection of claims 1,2,5, 7 – 9, 12, 14, 15 – 22, 23, 26 and 28 (Gupta in view of Hellestrand):

Applicant has argued that:

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. MPEP § 2142.

Applicant has also argued that the Gupta reference recites a methodology for embedded systems design. (Page 3, second paragraph). The objective of Gupta is to evaluate a range of target processors using an "application behavior specification" to determine the processors' suitability for use. (Page 3, Third paragraph).
Claim 1 recites a memory access monitor capable of "monitoring memory accesses to a simulated memory space" during "simulated execution" of a program, where the memory accesses include "read operations and write operations."

Applicant's arguments filed on February 12th 2004 have been fully considered but are moot in view of the new ground(s) of rejection that follows. [Please refer to Section 6].

The Examiner asserts that the *Gupta* reference is directed [**Pg 3, Chapter 1**] to a design methodology for embedded systems where given an application behavioral specification or characteristics, by following the methodology and with the help of the tools developed to support it, the user will be able to synthesize a system that meets the specification constraints

Drawings

3. **Figure 1** should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.1 **Claims 1 – 29** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Please refer to Regents of the University of California v. Eli Lilly & Co., 119 F.3d 1559, 1568, 43 USPQ2d 1398, 1405 (Fed. Cir. 1997); Hyatt v. Boone, 146F.3d 1348, 1354, 47 USPQ2d 1128, 1132 (Fed. Cir. 1998). Claim 1 drawn to an apparatus for designing a memory for use in an embedded system comprising:

- a simulation controller capable of simulating a program [line 3];
- a memory access monitor capable of monitoring memory access to a simulated memory space during execution of a program as well as generating memory usage statistics [line 6]; and
- a memory optimization controller capable of comparing memory usage statistical data and design criteria associated with the embedded system and determining at least one memory configuration capable of satisfying the design criteria.

There is not enough information on the specification or drawings of the instant application regarding these items.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5.1 The term "capable" in **independent claim 1** is a relative term, which renders the claim indefinite. The term "capable" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. As a result of this, the following claim limitations have been rendered indefinite: simulation controller [line 3], memory access monitor [line 6], and memory optimization controller [line 11]. **Claims 2 – 7** depend on independent claim 1 and therefore are rejected by virtue of their dependency on claim1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the

5, 12, 19 and 26

6.1 **Claims 1, 5, 6, 8, 12, 13, 15, 19, 20, 22, 26, 28 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over a printed publication by Gupta et al. (Inventor of instant application) titled "**Processor Evaluation in an Embedded Systems Design Environment**", hereafter referred to as Gupta, applied in view of a printed publication by Prete et al titled "**The ChARM Tool For Tuning Embedded Systems**", hereafter referred to as *Prete*.

6.1.1 Regarding **independent claims 1, 8, 15 and 22,** these claims are drawn to designing a memory for use in an embedded processing system comprising:

- simulating execution of a program to be executed by the embedded processing system;
- monitoring memory access, comprising read and write operations, during a simulated memory space during simulation of a program to be executed by the embedded processing system; and
- comparing memory usage statistical data and one or more design criteria associated with the embedded processing system, and determining a least one memory configuration capable of satisfying said one or more design criteria.

Gupta teaches [**Pg 3, Chapter** 1] synthesizing an architecture, for an embedded system that is best suited for a given application or program, that involves the identification of a set of parameters that characterize the processor architecture, developing an abstract model of the processor, extracting application parameters to capture the essential characteristics that must be present in the processor architecture [**Pg 23, 1st paragraph**]; carrying out a matching between the processor architecture and the given application (program). *Gupta* further teaches:

- Iterating (executing) over each function of the application (C Code) [**Pg 23, Chapter 5**]; and
- keeping track (monitoring) of the number of memory access I/O (read/write) operations during the iteration (execution) over all the instructions associated with a block of application code [**Pg26, section 5.4, last two paragraphs**].

The *Gupta* reference does not expressly teach comparing memory usage statistical data and one or more design criteria associated with the embedded processing system to determine at least one memory configuration capable of satisfying one or more design criteria.

The *Prete* reference teaches **[Pg 67, right Col, first paragraph]** a simulation tool that aids in building embedded systems by helping designers select the optimal system configuration (such as CPU speed, cache memory structure, system bus speed and main memory speed) to balance performance and cost. *Prete* also teaches **[Pg 68, right col., 2nd paragraph]** by simulating execution of applications to obtain sequence of memory operations produced by the executing program wherein each reference includes the address, the type of access performed (read or write), the area involved (data or code), and the number of clock cycles elapsed internal operations since the last memory operation. Additionally, *Prete* teaches **[Pg 70, last paragraph]** using traditional program statistic such as percentage of data, code, read, and memory reference patterns that affect performance to fine-tune the memory subsystem. The *Prete* reference further teaches **[Pg 67, left Col. first two paragraphs]** that design of embedded systems often involves balancing conflicting requirements (design criteria) for cost, die size, power consumption, processing power; designers must tune and optimize the system architecture to the particular embedded application by often turning to on-chip cache memories to provide both high processing power and the large main memory that some applications require; since cache memory keeps the off-chip memory bandwidth low this allows the use of slower – lower cost and lower power consumption – off-chip memory; cache memory does not furnish processing services to an application, however its presence and structure influence cost, system performance and power consumption and that "designers must answer fundamental questions such as is cache memory necessary to obtain the required application performance? If so, what is the optimal cache configuration? What configuration of the cache and main memory will satisfy the conflicting product requirements for performance, cost, and power consumption?".

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to modify the methodology for synthesizing an architecture for an embedded system as taught by *Gupta* to compare memory usage statistical data and one or more requirements or design criteria to determine at least one memory configuration that satisfies one or more design criteria in order to balance conflicting requirements (design criteria) for cost, die size, power consumption, processing power, tune and tailor the system architecture to the particular embedded application as taught by *Prete*.

6.1.2 As regards to **claims 5, 12, 19 and 26**, these claims are drawn to simulating the execution of a program N times, monitoring memory access during the execution, and generating memory usage statistics based on N executions of the program.

Gupta teaches **[chapter 7]** that the results generated by the parameter extractor are given for some functions from the mpeg code. The reference shows the histograms generated by the ASAP scheduler component on these functions. The histograms indicate some characteristics of the user program such as: percentage of cycles having a particular number of load/store operations, address computation operations and, data computational operations. The reference discloses that it can be noticed from the results that there is a lot of variation in all the parameter values.

Gupta does not expressly teach running the program N times.

Prete teaches **[Fig. 5 and corresponding text]** demonstration of system configuration tuning by specifying different requirements, such as percentage of miss ration and execution time, for different cache memory configurations that design of embedded.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to run the application program, as taught by *Gupta*, to tune the generated system configuration by running the application using different system configuration (N times) in order to obtain more run-time statistics about the user program and apply statistical analysis in order to reduce the variations in the parameter values as taught by *Prete*.

6.1.3 As regards **to claims 6, 13, 20 and 27**, these claims are drawn to determining at least one figure of merit associated with at least one memory configuration and wherein the at least one figure of merit indicates a degree to which said at least one memory configuration satisfies one or more design criteria;

Gupta teaches [**Chapter 7**] estimation results, which are output by the disclosed Estimator component, that show how parameters from the analyzed user program that can vary when compared to a range of target processors. The reference further discloses that the range of these parameters is substantial and can help in selecting/rejecting processors in performance critical application. Table 7.1 shows the results of the cycle count parameter and it is noted how there is a difference in the cycle count parameter (30% to 200%) between two different processors.

Gupta fails to explicitly teach performance results specific to memory configuration.

Prete teaches [**Pgs 70 – 72**] figures associated with at least one memory configuration and the degree to which the at least memory configuration satisfies one or more design criteria.

Therefore, it would have been obvious to one of ordinary skills in the art, at the time of the invention, to take the estimation results taught by *Gupta* to determine at least a memory configuration, which satisfies predetermined design criteria, as taught by *Prete*, along with a way of indicating the degree in which a memory configuration satisfies the predetermined design criteria to aid a designer in selecting/rejecting a particular processor architecture.

6.1.4 Regarding **claim 29**, this claim is drawn to generating memory usage statistical data comprising at least one of:

- one or more first histograms based on variable names contained in the program to be executed by the embedded processing system; and
- one or more second histograms based on memory locations accessed by the program to be executed by the embedded processing system.

Gupta teaches [Figs 7.2 – 7.12] generating Load/Store operations (read/write) histograms representing statistical data results for the different functions associated with a program to be executed by the embedded processing system.

Gupta does not expressly teach generating histograms to illustrate memory usage statistical data based on variable names contained in the program to be executed by the embedded system or memory locations accessed by said program.

Prete teaches the generation of histograms **[Fig 7]** to illustrate memory usage statistical data encompassing memory reference pattern (memory access) that affect the performance of an application, to be executed by the embedded processing system, also know as locality **[Pgs 70 – 71, Trace Analysis Phase section]**. *Prete* also teaches that an accurate knowledge of locality features plays a crucial role in fine-tuning the memory subsystem.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to modify the system taught by *Gupta* to generate memory usage statistical data results comprising of a histogram to illustrate the locality feature, for the program to

be executed by the embedded system, in order to fine-tune the memory subsystem configuration thus improving performance as taught by *Prete*.

6.2 **Claims 2 – 4, 7, 9 - 11, 14, 16 – 18, 21, 23 –25 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over a printed publication by Gupta et al. (Inventor of instant application) titled "**Processor Evaluation in an Embedded Systems Design Environment**", hereafter referred to as Gupta, applied in view of a printed publication by Prete et al titled "**The ChARM Tool For Tuning Embedded Systems**", hereafter referred to as *Prete* as applied above in further view of a printed publication by Dutt et al. titled "**Hot topic session: How to solve the current memory access and data transfer bottlenecks: at the processor architecture or at the compiler level?**" hereafter referred to as *Dutt*.

6.2.1 Regarding **Claims 2 - 4, 9 - 11, 16 –18 and 23 - 28, claims 2, 9, 16, and 23** are drawn to determining at least one memory configuration from a set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM) while **claims 3, 4, 10, 11, 17, 18, 24 and 25** are drawn to specifying at least one memory configuration comprising a first memory type and a first memory size, a second memory configuration comprising a second memory type and a second memory size. The limitations of claims **1, 8, 15 and 22** have been addressed in section 6.1.1 above.

Gupta teaches **[Pg 3, Chapter** 1] synthesizing an architecture, for an embedded system that is best suited for a given application or program, that involves the identification of a set of parameters that characterize the processor architecture, developing an abstract model of the processor, extracting application parameters to capture the essential characteristics that must be present in the processor architecture **[Pg 23, 1st paragraph]**; carrying out a matching between the processor architecture and the given application (program).

Gupta does not expressly teach the details of the identified processor architecture such as memory type and configuration.

Prete teaches **[Pg 67, left Col. first two paragraphs]** that design of embedded systems often involves balancing conflicting requirements (design criteria) for cost, die size, power consumption, processing power; designers must tune and optimize the system architecture to the particular embedded application by often turning to on-chip cache memories to provide both high processing power and the large main memory that some applications require since cache memory keeps the off-chip memory bandwidth low this allows the use of slower – lower cost and lower power consumption – off-chip memory; cache memory does not furnish processing services to an application, however its presence and structure influence cost, system performance and power consumption and that "designers must answer fundamental questions such as is cache memory necessary to obtain the required application performance? If so, what is the optimal cache configuration? What configuration of the cache and main memory will

satisfy the conflicting product requirements for performance, cost, and power consumption?".

Dutt teaches [section 2, first paragraph] that while microprocessor architectures have significantly evolved over the last fifteen years, the memory system is still a major bottleneck and **[section 4, 4th full paragraph]** that the only hope for achieving increasingly shorter time-to-market windows for memory-intensive systems, is a software toolkit generation approach, driven by an Architecture Description Language (ADL) which specifies the detailed processor architecture that including static (SRAM) and dynamic (DRAM) execution units and the detailed memory-subsystem architecture as well as any partitioning / mapping.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to modified the teachings of *Gupta* to include an ADL tool, as taught by *Dutt*, to specify detailed processor architecture that includes static (RAM or cache memory) and dynamic (DRAM or main memory) execution units that are tailored to the specific memory needs on an application in order to balance conflicting requirements (design criteria) for cost, die size, power consumption, processing power to allow designers to tune and optimize the system architecture to the particular embedded application as taught by *Prete*.

6.2.2 As regards to **claims 7, 14, 21 and 28**, these claims are drawn to a code optimization controller capable of modifying a program in response to a comparison of memory usage statistical data and one or more design criteria to thereby enable an

embedded processing system to execute the program according to one or more design criteria.

Gupta teaches [**Pg 8, section 3.1**] that the Stanford University Intermediate Format (SUIF) system is organized as a set of compiler passes built on top of a kernel that defines the intermediate representation, for a program, design to support both high-level program restructuring transformations as well as low-level analyses and optimizations.

Gupta does not expressly teach using the SUIF system's program transformation and optimization features to modify a program in response to a comparison of memory usage statistical data and one or more design criteria.

Prete teaches [**Pgs 67, right col**]a simulation tool that aids in building embedded systems by helping designer investigate how to improve performance by making small changes to the source code or to the memory mapping of a program.

Dutt teaches [**Pg 4, Fig 2 and corresponding text**] that decisions made in a "precompilation" stage heavily influence the final outcome of conventional compilers, when the internal organization of the SDRAM and embedded memories are correctly incorporated.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to tailor the SUIF system as taught by *Gupta* to improve performance of a program by making small changes to its source code or memory mapping, as taught by *Prete* in response to the incorporation of the internal organization of the SRAM and

embedded memories as taught by *Dutt* in order to help designers improve the performance of a given program or application.

Conclusion

7. Claims 1-29 have been reviewed for consideration as presented in Applicant's last correspondence.

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- *Gupta, T.V.K.; Sharma, P.; Balakrishnan, M.; Malik, S.;"* **Processor evaluation in an embedded systems design environment",** VLSI Design, 2000. Thirteenth International Conference on , 3-7 Jan. 2000, Pages:98 - 103
- *Sudhakar, P. Rama; Kumar, Shashi; "***Specification of Architecture Template for Embedded System Design***", Department of Computer Science and Engineering Indian Institute of Technology, Deli; December 1999.*
- *Progress Report for* **"ASSET: Automated SynthesiS of Embedded Systems A methodology for Heterogenous Implementations of Real Time Embedded Systems for Vision/Image Processing***", Department of Computer Science and Engineering Indian Institute of Technology, Deli; July 1999 -December 1999.*
- *Panda, P.R.; Dutt, N.D.; Nicolau, A.;"* **Local memory exploration and optimization in embedded systems",** Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 1 , Jan. 1999, Pages:3 - 13
- *Abraham, S.G.; Mahlke, S.A.;"* **Automatic and efficient evaluation of memory hierarchies for embedded systems",** Microarchitecture, 1999. MICRO-32. Proceedings. 32nd Annual International Symposium on , 16-18 Nov. 1999, Pages:114 - 125

- *Gries, M.;"* **The impact of recent DRAM architectures on embedded systems performance",** Euromicro Conference, 2000. Proceedings of the 26th , Volume: 1 , 5-7 Sept. 2000, Pages:282 - 289 vol.1
- *Kuulusa, M.; Nurmi, J.; Takala, J.; Ojala, P.; Herranen, H.;"***A flexible DSP core for embedded systems",** Design & Test of Computers, IEEE , Volume: 14 , Issue: 4 , Oct.-Dec. 1997, Pages:60 - 68
- *Shackleford, B.; Yasuda, M.; Okushi, E.; Koizumi, H.; Tomiyama, H.; Yasuura, H.;"* **Memory-CPU Size Optimization For Embedded System Designs",** Design Automation Conference, 1997. Proceedings of the 34th , June 9-13, 1997, Pages:246 - 251
- *Danckaert, K.; Catthoor, F.; De Man, H.;"* **System level memory optimization for hardware-software co-design",** Hardware/Software Codesign, 1997. (CODES/CASHE '97), Proceedings of the Fifth International Workshop on , 24-26 March 1997, Pages:55 - 59
- *Halambi, A.; Grun, P.; Ganesh, V.; Khare, A.; Dutt, N.; Nicolau, A.;* "**EXPRESSION: a language for architecture exploration through compiler/simulator retargetability",** Design, Automation and Test in Europe Conference and Exhibition 1999. Proceedings , 9-12 March 1999, Pages:485 - 490
- *Panda, P.R.; Dutt, N.D.; Nicolau, A.;"***Architectural exploration and optimization of local memory in embedded systems**", System Synthesis, 1997. Proceedings., Tenth International Symposium on , 17-19 Sept. 1997, Pages:90 - 97

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Morella Rosales-Hanner whose telephone number is (703) 305-8883. The examiner can normally be reached Monday-Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH

May 11, 2004